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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,910	01/03/2001	Odutola Oluseye Ewedemi	M-9129 US	5038

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EXAMINER	
WILSON, JACQUELINE B	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,910	EWEDEMI ET AL.	
	Examiner	Art Unit	
	Jacqueline Wilson	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13-21*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-17* is/are allowed.

6)☒ Claim(s) *13 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see amendment/remarks, filed 11/12/04, with respect to the rejection(s)of claim(s) 13-21 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Perner (US 6,552,745).

Please see new ground of rejection below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 13 is rejected under 35 U.S.C. 102(e) as being anticipated by Perner (US 6,552,745).

Regarding Claim 13, Perner teaches a sensor array including a two-dimensional array of pixel elements, that outputs digital signals as pixel data representing an image of a scene (shown in fig. 4, element 172; col. 2, lines 15+), and a dual-port data memory (col. 3, lines 62+), a first port of the dual-port data memory coupled to the sensor array (each dual port DRAM is coupled to each pixel, see abstract) for storing the pixel data

and a second port for exporting the pixel data (referred to as read bit line 14 and write bit line 12), the dual-port data memory being fabricated with the sensor array on a same integrated circuit (the memory and pixel are located on the same circuit as shown figs. 1-4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner'745 in view of Morris (US 6,697,112).

Regarding Claim 18, Perner teaches capturing an image of a scene using a sensor array (see fig. 4), storing pixel data representative of the images in a data memory being fabricated on a same integrated circuit as the sensor array (the memory and pixel are located on the same circuit as shown figs. 1-4), wherein the data memory is configured using a first memory interface protocol (referred to as write operations, col. 4, lines 30-35), outputting the pixel data to an image processing device (inherent since the device reads data out of the memory) outside of the integrated circuit using a second memory interface protocol (referred to as read operation, col. 4, lines 30-35), and receiving the pixel data at the image processing device using the second memory interface protocol (also inherent since an outside processor must be compatible with

transmission of the image data). However, Perner does not specifically disclose the image processing device is formed on an integrated circuit separate from the integrated circuit on which the sensor array and data memory are formed. Although this feature is notoriously well known in the art, a reference will be supplied. Morris et al is an example of how an image processing device (fig. 1, computer 14) having an integrated circuit is separate from the integrated circuit on which the sensor is arranged. The purpose of using separate circuit chip in different devices is for the purpose of recreating the image for display (col. 1, lines 30+). Therefore, it would have been obvious to one having ordinary skill in the art to further include an image processing device formed on an integrated circuit separate from the integrated circuit on which the sensor array and data memory are formed.

Regarding Claim 20, Perner teaches the two separate paths for the write and read operations allows for independent rates and/or independent processes for writing and reading data to and from an array of dual port DRAM cells.

6. Claims 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner'745, Morris (US 6,697,112), in view of Shepherd et al (US 6,434,665)

Regarding Claims 19 and 21, Perner teaches the two separate paths for the write and read operations allows for independent rates and/or independent processes for writing and reading data to and from an array of dual port DRAM cells, but fails to specifically teach the second memory interface protocol is a SRAM interface protocol or a packet protocol synchronous DRAM interface protocol. However Shepherd et al

teaches it is well known in the art to have memory interfaces able to convert between different frequencies (col. 3, lines 49+). Shepherd et al discloses a memory interface (120) that transfers data from a memory cache subsystem (136) to an external memory (108). These two memory locations operate at different frequencies (depending on whether the memory is SRAM, SDRAM or DRAM; col. 3, lines 34+) in which the bus transfers data. The memory interface is capable of converting the frequency of the data to the desired frequency of the target location for the purpose of properly storing data. Therefore, it would have been obvious to use the teaching of Shepherd et al in the device of Perner for converting the image data into the proper protocol according to the receiving location (such as using a SRAM or packet protocol synchronous DRAM interface).

Allowable Subject Matter

7. Claims 14-17 are allowed.

The prior art neither teaches nor fairly suggests an imaging system comprising an image sensor comprising a sensor array, including a two-dimensional array of pixel elements, that outputs digital signals as pixel data representing an image of a scene, a data memory coupled to the sensory array and fabricated with the sensor array on a first integrated circuit, the data memory for storing the pixel data, wherein the data memory is configured using a first memory interface protocol, **a logic circuit coupled to the data memory and fabricated with the data memory on the first integrated circuit, the logic circuit for accessing the data memory using the first memory**

interface protocol and performing memory interface conversion to provide an output memory interface configured using a second memory interface protocol different than the first memory interface protocol for exporting the pixel data out of the integrated circuit, and an image processing device formed on a second integrated circuit separate from the first integrated circuit and including a memory interface port configured using the second memory interface protocol, wherein the image sensor is coupled to the memory interface port of the image processing device and the image processing device accesses the pixel data in the image sensor using the second memory interface protocol.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacqueline Wilson whose telephone number is (571) 272-7322. The examiner can normally be reached on 8:30am-5:00pm (alternate Fridays off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (571) 272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JW
04/25/05

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